REMARKS

Claims 1-6 are pending upon entry of this amendment. Claims 1-5 have been amended and new claim 6 has been added. No new matter has been presented.

Claims 1-4 stand rejected under 35 USC 103(a) over Matsuzaki, U.S. Patent No. 6,088,255, in view of Kondo, U.S. Patent No. 6,417,706. This rejection is respectfully traversed.

Claim 1, as amended, recites "a first signal generator configured to set a first signal during a clock cycle of an internal clock during an initialization mode at a start of a burst." Claim 1 also has been amended to recite "the variable delay addition circuit receiving the first signal, detecting a duration time of the logic '1' of the first signal until the end of the clock cycle of the internal clock, and setting an initial value of the delay amount based on the duration time of the logic '1' of the first signal." These features are not taught or suggested by the combination of Matsuzaki and Kondo.

In rejecting claim 1, the Office Action merely asserts that several features are inherent in the structure of Matsuzaki's Figure 11 without providing any rational or explanation its assertion. Specifically, the Examiner asserts that the claimed features "[setting] first signal during a clock cycle of an internal clock" and "[detecting] a duration time of the first signal until the end of the clock cycle of the internal clock" are inherently present in Matsuzaki. Applicants respectfully disagree.

"In relying upon the theory of inherency, the ***examiner must provide a basis in fact and/or technical reasoning*** to reasonably support the determination that the allegedly inherent characteristic ***necessarily*** flows from the teachings of the applied prior art." Ex parte Levy, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990) (emphasis added). "The extrinsic evidence must make clear that the missing descriptive matter is ***necessarily present*** in the thing described in the reference, and that it would be so recognized by persons of ordinary skill." *In re Robertson*, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999) (emphasis added). The Examiner

provides no rationale or reasoned factual explanation as to why Matsuzaki's Figure 11 necessarily includes a first signal that is set during a clock cycle of an internal clock. In fact, Figure 11 of Matsuzaki does not show any structure generating such first signal. Further, the Examiner fails to provide any rationale or explanation as to why the variable delay circuits 210, 220 of Matsuzaki necessarily detect "a duration time of the first signal until the end of the clock cycle of the internal clock" and set "an initial value of the delay amount based on the duration time of the first signal." In fact, Matsuzaki makes clear that variable delay circuits 210, 220 use a ***predetermined*** phase delay, instead of a variable delay amount whose initial value is set based on the duration time of the logic '1' of another signal, to delay the external clock CLK. See Matsuzaki, Col. 15, lines 49-50. The mere fact that the initial value of the claimed delay amount is set based on another signal indicates that it does not have a predetermined amount. Accordingly, not only the claimed features of the invention are not inherently present in Matsuzaki's structure, the claimed features are clearly absent from Matsuzaki.

Kondo fails to overcome the deficiencies of Matsuzaki in teaching these features. Accordingly, claim 1 is allowable. Claim 2 recites similar features as claim 1, and claims 3-4 depend from claim 1. Thus, claims 2-4 are also allowable.

In view of the above, each of the claims in this application is in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue. If it is determined that a telephone conference would expedite the prosecution of this application, the Examiner is invited to telephone the undersigned at the number given below.

In the event the U.S. Patent and Trademark Office determines that an extension and/or other relief is required, applicants petition for any required relief including extensions of time and authorize the Commissioner to charge the cost of such petitions and/or other fees due in connection

with the filing of this document to **Deposit Account No. 03-1952** referencing docket no. **559502005500**.

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Respectfully submitted,

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